Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method comprising:

determining utilization values for a plurality of processors having power utilization dependencies; ~~and~~

identifying a target frequency for the plurality of processors based on the utilization values; and

transitioning a processor package including the plurality of processors to the target frequency, wherein the target frequency comprises a higher frequency if any of the utilization values is an up transition decision, and the target frequency comprises a lower frequency if all of the utilization values are a down transition decision.

Claim 2 (cancel)

Claims 3-5 (canceled)

Claim 6 (currently amended): The method of claim [[2]] 1, wherein identifying the target frequency comprises identifying a frequency operating point closest to a maximum operating frequency of the processor package multiplied by a maximum utilization of one of the plurality of processors having a highest value for the maximum utilization.

Claim 7 (cancel)

Claim 8 (cancel)

Claim 9 (original): The method of claim 1, wherein the plurality of processors comprise a plurality of logical processors.

Claim 10 (original): The method of claim 1, wherein the plurality of processors comprise at least one multicore processor.

Claim 11 (currently amended): A method comprising:

determining utilization decisions for logical processors of a physical processor using parameter information; and

calculating a target frequency for the physical processor based on the utilization decisions via combining the utilization decisions according to a first algorithm to obtain a first target frequency for the physical processor in a first operation mode, and combining the utilization decisions according to a second algorithm to obtain a second target frequency for the physical processor in a second operation mode.

Claim 12 (currently amended): The method of claim 11, further comprising transitioning the physical processor to ~~the~~ one of the first or second target ~~frequency~~ frequencies.

Claim 13 (original): The method of claim 11, further comprising transitioning the physical processor to a higher frequency if any of the logical processors has an up utilization decision.

Claim 14 (original): The method of claim 13, wherein the higher frequency is based on a highest utilization processor of the logical processors.

Claim 15 (original): The method of claim 11, further comprising transitioning the physical processor to a lower frequency if all of the logical processors have a down utilization decision.

Claim 16 (original): The method of claim 15, wherein the lower frequency is based on a highest utilization processor of the logical processors.

Claim 17 (original): The method of claim 12, wherein transitioning the physical processor comprises transitioning to a higher frequency if any of the logical processors needs additional compute power.

Claim 18 (original): The method of claim 11, wherein calculating the target frequency is based on desired power and performance characteristics.

Claim 19 (currently amended): An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

determine utilization values for a plurality of processors having power utilization dependencies, wherein the utilization values comprise an up transition decision or a down transition decision for each of the plurality of processors; and

identify a target frequency for the plurality of processors based on an aggregation of the utilization values.

Claim 20 (original): The article of claim 19, further comprising instructions that if executed enable the system to transition a processor package to the target frequency, the processor package including the plurality of processors.

Claim 21 (original): The article of claim 20, further comprising instructions that if executed enable the system to identify a frequency operating point closest to a maximum operating frequency of the processor package multiplied by a maximum utilization of one of the plurality of processors having a highest value for the maximum utilization.

Claim 22 (original): The article of claim 20, further comprising instructions that if executed enable the system to transition the processor package to a higher frequency if any of the plurality of processors needs additional compute power.

Claim 23 (original): The article of claim 20, further comprising instructions that if executed enable the system to transition the processor package to a lower frequency if any of the plurality of processors needs less power.

Claim 24 (previously presented): A system comprising:

a plurality of processors; and

a dynamic random access memory containing instructions that if executed enable the system to determine utilization values for the plurality of processors and to aggregate the utilization values to obtain a target frequency at which to operate the plurality of processors based on the aggregated utilization values.

Claim 25 (original): The system of claim 24, wherein the plurality of processors comprises a plurality of logical processors within a processor package.

Claim 26 (previously presented): The system of claim 25, further comprising instructions that if executed enable the system to obtain the target frequency corresponding to a frequency operating point closest to a maximum operating frequency of the processor package multiplied by a maximum utilization of one of the plurality of logical processors having a highest value for the maximum utilization.

Claim 27 (previously presented): The system of claim 25, further comprising instructions that if executed enable the system to transition the processor package to a higher frequency if any of the plurality of logical processors needs additional compute power.

Claim 28 (previously presented): The method of claim 1, wherein the plurality of processors have frequency transition dependencies.

Claim 29 (cancel)

Claim 30 (previously presented): The article of claim 19, wherein the plurality of processors have frequency transition dependencies.

Claim 31 (new): The method of claim 1, further comprising determining the utilization values for the plurality of processors in a selected one of the plurality of processors.

Claim 32 (new): The method of claim 1, further comprising determining the up transition decision for a corresponding one of the plurality of processors having a usage level greater than a first threshold.

Claim 33 (new): The method of claim 32, further comprising determining the down transition decision for a corresponding one of the plurality of processors having a usage level lower than a second threshold.